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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
STEVENS, ROBERTA A	

ART UNIT	PAPER NUMBER
2665	

DATE MAILED: 09/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/770,937	SANGHA ET AL.	
	Examiner	Art Unit	
	Roberta A Stevens	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 January 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1- 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Robins (U.S. 6430184 B1) in view of Runaldue (U.S. 6233244 B1).

4. Regarding claim 1, Robins teaches (figs 1, 3 and 6) a buffer management system for managing communication packets received from multiple I/O ports, comprising: on chip memory storing at least a free data pointer and a buffer descriptor (fig 1); the buffer descriptor including at least a data pointer pointing to a data buffer configured to store one or more or a portion of the communication packet (figure 6).

5. Robins does not teach the free pointer pointing to a buffer allocated in external memory; and the on chip memory having a maximum threshold such that if the number of buffer descriptors stored in the on-chip memory reaches the maximum, one or more descriptors stored in the on-chip memory are transferred to an external memory.

6. Runaldue teaches (col. 9, lines 13-39 and figure 4) a free pointer pointing to a buffer allocated in external memory; and the on chip memory having a maximum threshold such that if the number of buffer descriptors stored in the on-chip memory reaches the maximum, one or more descriptors stored in the on-chip memory are transferred to an external memory. It would have been obvious to one of ordinary skill in the art to adapt to Robins' system an external buffer to avoid data loss within the system.

7. Regarding claim 2, Robins teaches (fig 3) when one or more portions is received, a free data pointer is remover from the on-chip memory, the portion is stored in a data buffer pointed to by the free pointer; a buffer descriptor is generated including the free data pointer; and the descriptor is stored in the on-ship memory (col. 6, line 24 – col. 7, line 7).

8. Regarding claim 3, Robins does not teach one or more free pointers are stored in external memory; and the on-chip memory has a minimum threshold for the number of free data pointers stored in the on-chip memory such that if the minimum threshold is met one or more free data pointers are transferred from the external memory to the on-chip memory.

9. Runaldue teaches (col. 10, lines 8-13) one or more free pointers are stored in external memory; and the on-chip memory has a minimum threshold for the number of free data pointers

stored in the on-chip memory such that if the minimum threshold is met one or more free data pointers are transferred from the external memory to the on-chip memory. It would have been obvious to one of ordinary skill in the art to adapt to Robins system the transfer of portions from the overflow to the on-chip memory to maintain as much as possible high performance with in the system.

10. Regarding claim 4, Runaldue teaches (col. 10, lines 8-13) a direct memory access controller for transferring buffer descriptors between on-chip memory and external memory.

11. Regarding claim 5, Runaldue teaches (col. 9, line 13 – col. 10 and fig 4) the on-chip memory includes a read free queue where one or more free data pointers are stored.

12. Regarding claim 6, Robins teaches (figs 2A and 30) the on-chip memory includes a receive ready queue wherein one or more buffer descriptors is stored.

13. Regarding claims 7 and 22, Robins teaches (figs 2A and 33) the on-chip memory includes a transmit ready queue associated with an I/O port wherein one or more buffer descriptors generated for a communication packet destined for the I/O port are transferred from the receive ready queue to the transmit ready queue for the I/O port.

14. Regarding claim 8, Robins teaches (col. 16, line 17 – col. 17, line 45) the on-chip memory includes a write free queue for storage of a freed data pointer after the communication packet associated with that data pointer is transmitted.

15. Regarding claim 9, Robins teaches (col. 20, line 39 – col. 22) a plurality of transmit ready queues associated with a plurality of I/O ports, wherein transmission priority of communication packets is programmable based on the priority assigned to de-queuing buffer descriptors stored in the transmit ready queue.

16. Regarding claims 10, 23, 24 and 28-30, Runaldue teaches (fig 10) the on-chip memory comprises a receive ready queue for storing one or more buffer descriptors, including a writ FIFO and a read FIFO; wherein: newly generated buffer descriptors for received communication packets are written to the write FIFO; buffer descriptors written to the write FIFO are moved to the read FIFO, if the read is below a maximum threshold level; otherwise buffer descriptors written to the write FIFO are transferred to the external memory and are moved to the read FIFO if I it is below a maximum threshold level.

17. Regarding claim 11, Robins teaches (figs 1, 3 and 6) a method for receiving communication packets in a communication system using a buffer management system, comprising: storing in a data buffer one or a portion of a communication packet receive by an I/O port; generating a buffer descriptor including at least the data pointer; storing the buffer descriptor in an on-chip receive ready queue.

18. Robins does not teach the free pointer pointing to a buffer allocated in external memory; and the on chip memory having a maximum threshold such that if the number of buffer descriptors stored in the on-chip memory reaches the maximum, one or more descriptors stored in the on-chip memory are transferred to an external memory.

19. Runaldue teaches (col. 9, lines 13-39 and figure 4) a free pointer pointing to a buffer allocated in external memory; and the on chip memory having a maximum threshold such that if the number of buffer descriptors stored in the on-chip memory reaches the maximum, one or more descriptors stored in the on-chip memory are transferred to an external memory. It would have been obvious to one of ordinary skill in the art to adapt to Robins' system an external buffer to avoid data loss within the system.

20. Regarding claims 12 and 32, Robins teaches (fig 6) the buffer descriptor is generated if end of a communication packet is detected.

21. Regarding claims 13 and 33, Robins teaches (fig 6) the buffer descriptor is generated if the data buffer is full.

22. Regarding claims 14, 26 and 34, Robins teaches (fig 6) if the receive ready queue is not empty then a processor reading a buffer descriptor from the receive ready queue.

23. Regarding claims 15, 25, 35 and 44, Runaldue teaches (col. 10, lines 8-13) if the receive ready queue reaches a maximum threshold then transferring one or more buffer descriptors, if any, from the external memory to the receive ready queue.

24. Regarding claims 16 and 36, Robins teaches (figs 2A and 30) the processor processing one or more descriptor fields in the buffer descriptor.

25. Regarding claim 17, Robins teaches (figs 26-28 and 35-35A) one of the descriptor fields is a length field.

26. Regarding claim 18, Robins teaches (figs 26-28) one of the descriptor fields is a status field indicating error free status.

27. Regarding claim 19, Robins teaches (figs 26-28) one of the descriptor fields is a type field indicating storing the beginning, middle or end of a packet.

28. Regarding claims 20 and 37, Robins teaches (fig 7A) one of the descriptor fields is a destination field indicating the destination of one or more portions of the packet.

29. Regarding claim 21, Robins teaches (fig 1A) the processor determining the destination of transmission of the packet.

30. Regarding claims 27 and 38, Robins teaches (fig 1A) the destination I/O port transmitting the packet to the destination node based on the destination information stored in the BD.

31. Regarding claim 31, Robins teaches (figs 1, 3 and 6) a method for managing communication packets using a buffer management system, comprising: storing in a data buffer one or a portion of a communication packet constructed by a software application; generating a buffer descriptor including at least the data pointer; storing the buffer descriptor in an on-chip receive ready queue.

32. Robins does not teach a read free queue having a minimum threshold, the data pointer pointing to a buffer allocated in external memory the on chip memory having a maximum threshold such that if the number of buffer descriptors stored in the on-chip memory reaches the maximum, one or more descriptors stored in the on-chip memory are transferred to an external memory.

33. Runaldue teaches (col. 9, lines 13-39 and figure 4) a read free queue having a minimum threshold, the data pointer pointing to a buffer allocated in external memory the on chip memory having a maximum threshold such that if the number of buffer descriptors stored in the on-chip memory reaches the maximum, one or more descriptors stored in the on-chip memory are transferred to an external memory. It would have been obvious to one of ordinary skill in the art to adapt to Robins' system an external buffer to avoid data loss within the system.

34. Regarding claim 39, Robins teaches (fig 1A) I/O port reading the buffer descriptor from on-chip transmit ready queue

35. Regarding claim 40, Runaldue teaches (fig 10) I/O port returning the data pointer associated with the buffer descriptor to an on-chip write free queue.

36. Regarding claim 41, Robins teaches (figs 1, 3 and 6) a method for managing interleaved communication streams in a communication system comprising: generating a buffer descriptor having type and status data; the type data indicating whether the buffer descriptor is associated with a data buffer that stores beginning, middle, and end of a communication packet; the status data indicating the communication channel from which the packet was received (figs. 26-28 and 35-35A); storing the buffer descriptor in on-chip memory; reading the buffer descriptors from the on-chip memory; examining the type data for the buffer descriptor; and if the type data indicates that a buffer descriptor is associated with a data buffer that stores the end of a packet then notifying higher layer application that a packet is received (fig. 6).

37. Robins does not teach moving the buffer descriptor from on-chip memory to a buffer in external memory associated with the communication channel identified by the status data.

38. Runaldue teaches (col. 9, lines 13-39 and figure 4) moving the buffer descriptor from on-chip memory to a buffer in external memory associated with the communication channel identified by the status data. It would have been obvious to one of ordinary skill in the art to adapt to Robins' system an external buffer to avoid data loss within the system.

39. Regarding claim 42, Robins teaches (figs 1, 3 and 6) in a communication system, a buffer management system for managing packets received from multiple I/O ports, comprising: a first

memory for storing at least a free data pointer and a buffer descriptor; the buffer descriptor including at least a data pointer pointing to a data buffer configured to store one or a portion of the packet

40. Robins does not teach a free data pointer pointing to a buffer allocated in a second memory; and if the number of buffer descriptors stored in the first memory reaches a maximum threshold transferring one or more descriptors to the second memory.

41. Runaldue teaches (col. 9, lines 13-39 and figure 4) a free data pointer pointing to a buffer allocated in a second memory; and if the number of buffer descriptors stored in the first memory reaches a maximum threshold transferring one or more descriptors to the second memory. It would have been obvious to one of ordinary skill in the art to adapt to Robins' system an external buffer to avoid data loss within the system.

42. Regarding claim 43, Runaldue teaches (col. 9, lines 13-39) the first memory is accessible faster than the second memory.

Claim Objections

43. The numbering of claims is not in accordance with 37 CFR 1.126 which requires the original numbering of the claims to be preserved throughout the prosecution. When claims are canceled, the remaining claims must not be renumbered. When new claims are presented, they must be numbered consecutively beginning with the number next following the highest numbered claims previously presented (whether entered or not).

44. Misnumbered claims 43-43 have been renumbered 43-44.

Conclusion

1. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Roberta A Stevens whose telephone number is 571-272-3161. The examiner can normally be reached on M-F 9:00am-5:30pm.

2. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on 571-272-3155. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

3. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Roberta A Stevens
Examiner
Art Unit 2665

STEVEN NGUYEN
PRIMARY EXAMINER